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10/538,457	06/10/2005	**Carl Knudsen**	US02 0612 US	3800

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EXAMINER	
SQUIRES, BRETT S	

ART UNIT	PAPER NUMBER
2431	

NOTIFICATION DATE	DELIVERY MODE
05/28/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/538,457	KNUDSEN, CARL	
	Examiner	Art Unit	
	BRETT SQUIRES	2431	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 June 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Drawings

1. The drawings are objected to because text labels are necessary for the applicant's drawings to be understood. The drawings in a nonprovisional application must show every feature of the invention specified in the claims. See 37 CFR 1.83(a). Figure 2 contains rectangular boxes whose meanings are unclear instead of conventional drawing symbols whose meanings are readily apparent, such as the circuit elements that represent resistors, capacitors, or inductors. Accordingly, the rectangular boxes should have text labels for clarification purposes.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-2, 8-12,15-17, and 19-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Kommerling et al. (US 7,005,733).

Regarding Claim 1, 15-16, and 19-20:

Kommerling discloses an integrated circuit device ("Integrated Circuit of Microchip," See fig. 1b ref. no. 195 and col. 6 lines 24-30) having a plurality of magnetically-responsive circuit nodes ("Hall Effect Sensors" See figs. 1a, 1b, 5a, and 5b ref. no. 150 and "Another is to allocate to each sensor a one bit value indicating whether it's reading exceeds a threshold (derived initially based on the statistics of the readings) or not." See col. 9 lines 46-48), a package adapted to inhibit access to the integrated circuit device ("The encapsulation 50 surrounds the device substrate 350 on both sides and comprises an epoxy resin matrix." See col. 10 lines 44-52) and including a plurality of magnetized particles therein ("Within the matrix, a plurality of particles 360 are provided, of various sizes, shapes and/or magnetic permeabilities." See col. 10 lines 44-52), the magnetically-responsive circuit nodes magnetically responding to the plurality of magnetized particles such that a change in magnetic field collectively provided by the

magnetized particles renders a change in a magnetic state of at least one of the magnetically-responsive circuit nodes ("Thus, magnetic properties measured by the sensors 150 will generally be different at each of the sensors, as described above. Further, any attempt to remove the outer shield 370 will itself change the distribution of the magnetic field and therefore make it impossible to read the key." See col. 11 lines 4-6).

Regarding Claim 2:

Kommerling discloses the integrated circuit device includes a detection circuit adapted to detect the magnetic state of the magnetically-responsive circuit nodes ("Sense Amplifier" See fig. 3 ref. no. 300 and col. 9 lines 20-32) and in response to a change in the magnetic state, to detect that the package has been tampered with ("In the event of tampering with the encapsulation 50, the encapsulation properties 170 are altered, leading to alterations in the detected properties140 and hence the cryptographic input (key) 160." See col. 6 lines 17-23).

Regarding Claims 8-12:

Kommerling discloses the areas of the encapsulation 50 sensed by each sensor 150 may overlap or abut each other; the key criterion in order to prevent holes being drilled through the encapsulation to the circuit below, is that the areas sensed by the sensors leave no separation larger than the width of the smallest hole which can be drilled (for example using focused ion beam technology.

Regarding Claim 17:

Kommerling discloses a tamper-response circuit ("Linear Feedback Shift Register" See fig. 3 ref. no. 330) adapted to alter a characteristic of the integrated circuit chip in response to the tamper protection circuit detecting the magnetic response of the at least one magnetically-responsive elements ("The successive digital sensor readings are then loaded into a linear feedback shift register (LFSR) 330 which combines them according to some scrambling function and produces a key 340 of the requested length (e.g. 64 bits) using all sensor readings, in some logical combination." See col. 9 lines 33-37).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-7 and 14 are rejected under 35 U.S.C. 103(a) as being obvious over Sano (JP 3084959 A) in view of Kommerling et al. (US 7,005,733).

Regarding Claim 1 and 14:

Sano discloses an integrated circuit device ("Package" See fig. 2 ref. no. 4) having a plurality of magnetically-responsive circuit nodes ("Hall Element" See fig. 1 ref. no. 1), a magnet detachably connected to the integrated circuit device chip ("A magnet 5 is installed at the outside of the package so as to be freely detachable." See fig. 2 ref. no. 5 and abstract), the magnetically-responsive circuit nodes magnetically responding

to the magnet such that a change in magnetic field provided by the magnet renders a change in a magnetic state of at least one of the magnetically-responsive circuit nodes (A hall element 1 detects a magnetic field from the outside of a package of an integrated circuit." See abstract).

Sano does not disclose a plurality of magnetically-responsive circuit nodes and a package adapted to inhibit access to the integrated circuit device and including a plurality of magnetized particles therein.

Kommerling discloses an integrated circuit having a hall effect sensors disposed covering all circuit-containing areas (See col. 9 lines 54-56 and col. 10 lines 2-11) and an encapsulation surrounding a device substrate on both sides and comprises an epoxy resin matrix. Within the matrix are a plurality of particles of various sizes, shapes and/or magnetic permabilities. A pair of plate shaped permanent magnets are provided above and below the encapsulation layers and bonded thereto by the epoxy resin. (See col. 10 lines 44-58).

It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the detachable magnet disclosed by Sano with the epoxy resin matrix and permanent magnets and includes hall effect sensors disposed covering all circuit-containing areas such as those taught by Kommerling in order to protect the integrated circuit device from tampering (See Kommerling col. 2 lines 17-20 and col. 10 lines 2-11).

Regarding Claim 2:

The above stated combination of Sano and Kommerling discloses the integrated circuit arrangement includes a detection circuit adapted to detect the magnetic state of the magnetically-responsive circuit node ("The mode changeover circuit 2 instructs a mode changeover by a magnetic-field detection output from the Hall element 1." See Sano fig. 1 ref. no. 2 and abstract) and in response to a change in the magnetic state to detect that the package has been tampered with ("The mode changeover circuit 2 is connected to a circuit main body 3 and changes its operating mode by an input from the mode changeover circuit 2." See Sano abstract).

Regarding Claim 3:

The above stated combination of Sano and Kommerling discloses the detection circuit includes a comparison circuit adapted to compare the detected a magnetic state with a reference and to detect tampering with the package in response to the detected magnetic state being different than the reference state [The examiner respectfully points out that the mode changeover circuit inherently includes a comparison circuit with a reference voltage value. The hall element will output a first voltage to the mode changeover circuit when the magnet is installed at the outside of the package and output a second voltage to the mode changeover circuit when the magnet is removed from the outside of the package. The mode changeover circuit will receive the voltage output from the hall element and in order to determine if the magnet was removed must perform a comparison of the received voltage will a reference voltage value. For example, an integrated circuit having a default high mode changeover circuit using transistor transistor logic a comparison will be performed to determine if the received

voltage between 2.2v and 5v for a high (magnet installed) and 0v to 0.8v for low (magnet removed).]

Regarding Claims 4 and 5:

The above stated combination of Sano and Kommerling discloses an integrated circuit device having a the epoxy resin matrix and permanent magnets package and a mode changeover circuit that senses changes in the epoxy resin and permanent magnets package to detect tempering with the package.

The above stated combination of Sano and Kommerling does not disclose one-time programmable ROM adapted to store data representative of an untampered magnetic state of the magnetically-responsive node.

Kommerling discloses an integrated circuit device having an initialization circuit with a ROM storing a loader program that reader the detected property signal (See col. 6 lines 31-51)

It would have been obvious to one of ordinary skill in the art at the time of the invention to include in the above stated combination of Sano and Kommerling a initialization circuit with a ROM such as that taught by Kommerling in order to allow the manufacturer to set the voltage levels for determining when the package has been tampered with.

Regarding Claim 6:

The above stated combination of Sano and Kommerling discloses an integrated circuit device having a the epoxy resin matrix and permanent magnets package and a

mode changeover circuit that senses changes in the epoxy resin and permanent magnets package to detect tempering with the package.

The above stated combination of Sano and Kommerling does not disclose the integrated circuit device is adapted to alter data stored in the integrated circuit in response to the comparison circuit detecting tampering with the package.

Kommerling discloses an integrated chip that in the event of tampering with the encapsulation, the encapsulation properties are altered leading to alteration in the detected properties and hence the cryptographic key (See col. 6 lines 17-23).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the above stated combination of Sano and Kommerling to include altering data stored in the integrated circuit such as that taught by Kommerling in order to render to the device inoperative after the device has been tampered with (See Kommerling col. 6 lines 17-23).

Regarding Claim 7:

The above stated combination of Sano and Kommerling discloses the integrated circuit device is adapted to set a tamper-detection flag in response to the comparison circuit detecting tampering ("The mode changeover circuit 2 is connected to a circuit main body 3 and changes its operating mode by an input from the mode changeover circuit 2." See Sano abstract).

6. Claim 13 is rejected under 35 U.S.C. 103(a) as being obvious over Kommerling et al. (US 7,005,733) in view of Fujiki (JP 7209019 A).

Kommerling discloses the above stated an integrated circuit having a plurality of Hall Effect sensors and an epoxy resin and permanent magnets package to detect tempering with the package.

Kommerling does not disclose each magnetically-responsive circuit node includes a circuit element that resistively responds to a magnetic field generated by the magnetized particles.

Fujiki discloses a magnetic encoder having a magnetic resistance effect element (See fig. 1 ref. no. 1 and abstract) and an integrated circuit to treat signals output from the magnetic resistance effect element (See fig. 1 ref. no. 2 and abstract).

It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the Hall Effect sensors disclosed by Kommerling with the magnetic resistance effect element such as the taught by Fujiki in order to reduce the size of the magnetic signal detection processing part (See Fujiki abstract).

7. Claims 17-18 are rejected under 35 U.S.C. 103(a) as being obvious over Kommerling et al. (US 7,005,733) in view of Double et al. (US 5,129,629).

Kommerling discloses the above stated an integrated circuit having a plurality of Hall Effect sensors and an epoxy resin and permanent magnets package to detect tempering with the package.

Kommerling does not disclose a tamper-response circuit is adapted to erase memory from the integrated circuit chip in response to the tamper-protection circuit detecting the magnetic response of the at least one magnetically-responsive elements.

Double discloses an encryption/decryption circuit for detecting and prevent unauthorized interrogation that determines if any one of the sensor inputs changes from high to low, as a result of certain predetermined conditions indicating an attack the NAND gate will turn on and the data from memory will be quickly erased (See fig. 2, col. 3 lines 51-68 and col. 4 lines 1-15).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Kommerling to include erasing data from memory in response to an unauthorized interrogation such as that taught by Double in order to protect the contents of the computer memory from being unlawfully or unauthorizedly extracted and read (See Double col. 1 lines 16-18).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to BRETT SQUIRES whose telephone number is (571) 272-8021. The examiner can normally be reached on 9:30am - 6:00pm Monday - Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Korzuch can be reached on (571) 272-7589. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/BS/

/William R. Korzuch/
Supervisory Patent Examiner, Art Unit 2431